Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S142	6	S140 and (conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/23 08:19
S141	0	S140 and (conflict same position)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/23 08:19
S140	84	(fragment near3 shading)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/23 08:18
S138	151	(delay$3 or stall$3) same (position and fragment)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/23 08:18
S139	1	(delay$3 or stall$3) same (position and fragment and tile)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/23 08:17
S137	2	(delay$3 or stall$3) same (conflict and position and fragment)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/23 08:16
S136	9	S135 and "345"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/08/20 11:13
S135	123	tile adj state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/08/20 11:13
S134	9	345/564.ccls. and (fragment and tile)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/08/20 11:12
S133	210	345/564.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/08/20 10:12
S132	1	345/473.ccls. and ((stor$3 or sav$3) near3 (timestamp or (time adj3 stamp)))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:24
S131	8	345/475.ccls. and (time same (entry or slot))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:24
S130	3	345/475.ccls. and (time same (bin or tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:24

S127	94	345/473.ccls. and (time same (entry or slot))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:24
S76	1	345/473.ccls. and ((stor$3 or sav$3) near3 (timestamp or (time adj3 stamp)))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:24
S73	3	345/475.ccls. and (time same (bin or tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:24
S129	0	345/475.ccls. and ((timestamp or (time adj3 stamp)) near5 (bin or tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:23
S128	135	345/475.ccls.	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:23
S126	20	345/473.ccls. and (time same (bin or tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:23
S125	0	345/473.ccls. and ((timestamp or (time adj3 stamp)) near5 (bin or tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:23
S71	0	345/475.ccls. and ((timestamp or (time adj3 stamp)) near5 (bin or tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:23
S70	86	345/473.ccls. and (time same (entry or slot))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:23
S67	20	345/473.ccls. and (time same (bin or tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:23
S65	0	345/473.ccls. and ((timestamp or (time adj3 stamp)) near5 (bin or tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:23
S64	130	345/475.ccls.	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:23
S124	3	"345"/$.ccls. and (tile near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:22
S123	27	"345"/$.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:22
S122	0	345/545.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21
S121	0	345/582.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21

S120	0	345/423.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21
S119	0	345/614.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21
S118	3	345/614.ccls. and conflict$3	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21
S117	1	(S113 and S114) and (conflict$3 and tile)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21
S116	0	345/614.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:21
S105	0	345/423.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:21
S49	24	"345"/$.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21
S43	0	345/614.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21
S42	3	345/614.ccls. and conflict$3	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21
S40	1	(S37 and S38) and (conflict$3 and tile)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:21
S115	0	(S113 and S114) and (conflict$3 and tile and fragment)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:20
S114	200	382/306.ccls.	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:20
S113	718	382/305.ccls.	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:20
S112	0	345/545.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:20

S11 1	4	345/582.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:20
S11 0	1	345/426.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:20
S39	0	(S37 and S38) and (conflict$3 and tile and fragment)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/08/20 09:20
S23	0	345/423.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:20
S10 4	81	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:19
S22	76	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:19
S10 3	63	345/626.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:18
S19	54	345/626.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:18
S10 2	67	345/614.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:16
S18	56	345/614.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:16

S101	4	345/582.ccls. and (image near5 tile) and (fragment near5 shad$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:15
S17	4	345/582.ccls. and (image near5 tile) and (fragment near5 shad$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:15
S100	36	345/582.ccls. and (fragment and tile and shad$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:14
S99	741	345/582.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:14
S15	31	345/582.ccls. and (fragment and tile and shad$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:14
S14	670	345/582.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:14
S98	18	345/426.ccls. and (tile near5 (identi$4 or number or tag or label))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:11
S97	17	345/426.ccls. and (tile near7 image) and shad$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:11
S96	13	345/426.ccls. and (fragment and tile)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:11
S95	60	345/426.ccls. and fragment	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:08

S13	14	345/426.ccls. and (tile near5 (identi$4 or number or tag or label))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:08
S12	15	345/426.ccls. and (tile near7 image) and shad$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:08
S11	12	345/426.ccls. and (fragment and tile)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:08
S10	55	345/426.ccls. and fragment	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:08
S93	634	345/426.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:06
S9	576	345/426.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:06
S5	24	345/423.ccls. and fragment	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 09:06
S92	44	S90 not S91	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 07:56
S91	11	(fragment adj shad$3) and tile	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 07:56
S90	55	(fragment near3 shad$3) and tile	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 07:56

S87	18	345/423.ccls. and ((memor$3 or register$1 or storage) same tile)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 07:56
S3	9	(fragment adj shad$3) and tile	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/20 07:56
S89	10	345/423.ccls. and (tile near5 identif$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/19 15:03
S88	13	345/423.ccls. and (tile near5 number)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/19 14:11
S7	12	345/423.ccls. and ((memory or register) same tile)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/19 14:06
S85	27	345/423.ccls. and fragment	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/19 14:03
S84	418	345/423.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/19 14:03
S4	388	345/423.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/19 14:03
S83	11	(fragment adj shad$3) and tile	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/08/19 13:10
S82	10	montrym-john-s.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/08/19 13:10

S81	7	molnar-steven-e.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/08/19 13:08
S2	8	montrym-john-s.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/08/19 13:08
S1	6	molnar-steven-e.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2005/08/19 13:08
S80	19	token same S79	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/15 11:38
S79	497	(updat$5 or refresh$4) adj3 timestamp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/15 11:38
S78	7	"345"/$.ccls. and ((stor$3 or sav$3) near3 (timestamp or (time adj3 stamp)) and (tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/03/01 10:45
S77	60	"345"/$.ccls. and ((stor$3 or sav$3) near3 (timestamp or (time adj3 stamp)))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/03/01 10:44
S75	1	345/475.ccls. and ((stor$3 or sav$3) near3 (timestamp or (time adj3 stamp)))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/03/01 10:28
S74	8	345/475.ccls. and (time same (entry or slot))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/03/01 10:27
S72	0	345/475.ccls. and ((timestamp or (time adj3 stamp)) near5 (entry or slot))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/03/01 10:22
S68	0	345/473.ccls. and ((timestamp or (time adj3 stamp)) near5 (entry or slot))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/03/01 10:22
S69	0	345/473.ccls. and ((timestamp or (time adj3 stamp)) same (entry or slot))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/03/01 09:58
S66	0	345/473.ccls. and ((timestamp or (time adj3 stamp)) same (bin or tile))	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/03/01 09:36

S63	977	345/473.ccls.	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/03/01 09:35
S62	3	345/556.ccls. and (tile near3 state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/08 07:57
S61	1	345/552.ccls. and (tile near3 state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/08 07:57
S60	4	345/545.ccls. and (tile near3 state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/08 07:56
S57	5	345/582.ccls. and (tile near3 state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/08 07:56
S56	2	345/426.ccls. and (tile near3 state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/08 07:56
S59	0	345/626.ccls. and (tile near3 state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/08 07:55
S58	0	345/614.ccls. and (tile near3 state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/08 07:55
S55	3	345/423.ccls. and (tile near3 state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/08 07:55
S54	1	"382"/$.ccls. and ((position same conflict$3) and tile)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/08 07:48
S53	4	"345"/$.ccls. and ((position same conflict$3) and tile)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/08 07:46

S52	42	"382"/$.ccls. and ((timestamp or (time adj3 stamp)) and tile)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 10:27
S51	47	"345"/$.ccls. and ((timestamp or (time adj3 stamp)) and tile)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 10:13
S50	8	"382"/$.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 09:45
S48	0	345/545.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 09:38
S47	0	345/556.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 09:38
S46	0	345/582.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 09:34
S45	0	345/426.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 09:34
S44	0	345/423.ccls. and (position near7 conflict$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 09:34
S38	189	382/306.ccls.	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 09:25
S37	659	382/305.ccls.	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 09:17
S36	1	S34 and conflict$3	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/02/07 09:17
S34	7	(US-20030164830-$ or US-20040169650-$).did. or (US-6204856-$ or US-6424345-$ or US-6496193-$ or US-6717576-$ or US-6741247-$).did.	US-PGPUB; USPAT	OR	OFF	2005/02/07 08:30
S33	1	345/556.ccls. and (fragment and conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:55
S32	2	345/556.ccls. and (tile and conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:54

S31	0	345/556.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:53
S30	158	345/556.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:53
S21	137	345/543.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:53
S29	29	345/545.ccls. and ((memory or register) same tile)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:05
S27	16	345/545.ccls. and (tile near5 (identi$4 or number or tag or label))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:03
S26	2	345/545.ccls. and (image near5 tile) and (fragment near5 shad$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:03
S28	0	345/545.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:02
S25	4	345/582.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 14:00
S24	1	345/426.ccls. and (tile same conflict)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 13:59
S20	427	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 13:44

S16	2	"6373482".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 12:14
S8	1	345/423.ccls. and (fragment same (shadow or shaded or shade or shading)) and tile	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/02/03 08:51

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stall fragment conflict AND

AND

AND

AND

AND

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IPC --- e.g. D01B7/04 A01C11/02

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tile fragment conflict AND

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delay fragment conflict AND

AND

AND

AND

AND

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fragment conflict AND

AND

AND

AND

AND

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No.	Publication No.	Title
1.	2004 - 326678	RENDERING PROCESSING UNIT AND GRAPHICAL PROCESSING METHOD

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2004-326678

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(51)Int.Cl. G06T 15/00
G06T 17/40

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(22)Date of filing : 28.04.2003

(71)Applicant : TOSHIBA CORP

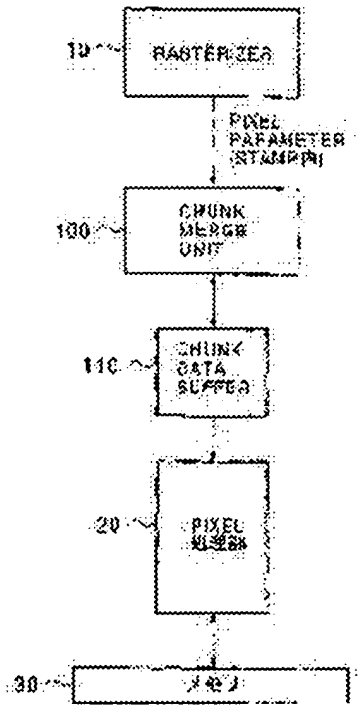
(72)Inventor : SAITO TAKAHIRO
MORI KENICHI

(54) RENDERING PROCESSING UNIT AND GRAPHICAL PROCESSING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a rendering processing unit with improved processing capability.

SOLUTION: A chunk merge unit 100 keeps on storing pixel data entered from a rasterizer 10 into a chunk data buffer 110 by the fragment termed a chunk, and when pixel data contained in the chunk of the same position as the chunk already stored in the chunk data buffer 110 are entered from the rasterizer 10, merges the two chunks if no conflict of pixel data occurs.



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1 Dynamically scheduled VLIW processors

B. Ramakrishna Rau

December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**

Full text available: pdf(1.64 MB) Additional Information: full citation, references, citings

Keywords: VLIW processors, dynamic scheduling, multiple operation issue, out-of-order execution, scoreboarding

2 Reducing instruction cache energy consumption using a compiler-based strategy

W. Zhang, J. S. Hu, V. Degalahal, M. Kandemir, N. Vijaykrishnan, M. J. Irwin

March 2004 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 1 Issue 1

Full text available: pdf(1.15 MB) Additional Information: full citation, abstract, references, index terms

Excessive power consumption is widely considered as a major impediment to designing future microprocessors. With the continued scaling down of threshold voltages, the power consumed due to leaky memory cells in on-chip caches will constitute a significant portion of the processor's power budget. This work focuses on reducing the leakage energy consumed in the instruction cache using a compiler-directed approach.We present and analyze two compiler-based strategies termed as conservative and optim ...

Keywords: Leakage power, cache design, compiler optimizations

3 Realizing OpenGL: two implementations of one architecture

Mark J. Kilgard

August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.66 MB) Additional Information: full citation, references, citings, index terms

Keywords: O2, OpenGL, graphics hardware architecture, infinite-reality

4 Application restructuring and performance portability on shared virtual memory and hardware-coherent multiprocessors

Dongming Jiang, Hongzhang Shan, Jaswinder Pal Singh

June 1997 **ACM SIGPLAN Notices , Proceedings of the sixth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 32 Issue 7

Full text available: pdf(1.59 MB) Additional Information: full citation, abstract, references, citings, index terms

The performance portability of parallel programs across a wide range of emerging coherent shared address space systems is not well understood. Programs that run well on efficient, hardware cache-coherent systems often do not perform well on less optimal or more commodity-based communication architectures. This paper studies this issue of performance portability, with the commodity communication architecture of interest being page-grained shared virtual memory. We begin with applications that per ...

5 Pomegranate: a fully scalable graphics architecture

Matthew Eldridge, Homan Igehy, Pat Hanrahan

July 2000 **Proceedings of the 27th annual conference on Computer graphics and interactive techniques**

Full text available: pdf(508.39 KB) Additional Information: full citation, abstract, references, citings, index terms

Pomegranate is a parallel hardware architecture for polygon rendering that provides scalable input bandwidth, triangle rate, pixel rate, texture memory and display bandwidth while maintaining an immediate-mode interface. The basic unit of scalability is a single graphics pipeline, and up to 64 such units may be combined. Pomegranate's scalability is achieved with a novel "sort-everywhere" architecture that distributes work in a balanced fashion at every stage of the pipeline, ke ...

Keywords: graphics hardware, parallel computing

6 Processor coupling: integrating compile time and runtime scheduling for parallelism

Stephem W. Keckler, William J. Dally

April 1992 **ACM SIGARCH Computer Architecture News , Proceedings of the 19th annual international symposium on Computer architecture**, Volume 20 Issue 2

Full text available: pdf(1.32 MB) Additional Information: full citation, abstract, references, citings, index terms

The technology to implement a single-chip node composed of 4 high-performance floating-point ALUs will be available by 1995. This paper presents processor coupling, a mechanism for controlling multiple ALUs to exploit both instruction-level and inter-thread parallelism, by using compile time and runtime scheduling. The compiler statically schedules individual threads to discover available intra-thread instruction-level parallelism. The runtime scheduling mechanism interleaves threads, explo ...

7 A fast and accurate framework to analyze and optimize cache memory behavior

Xavier Vera, Nerina Bermudo, Josep Llosa, Antonio González

March 2004 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 26 Issue 2

Full text available: pdf(270.06 KB) Additional Information: full citation, abstract, references, index terms, review

The gap between processor and main memory performance increases every year. In order to overcome this problem, cache memories are widely used. However, they are only effective when programs exhibit sufficient data locality. Compile-time program transformations can significantly improve the performance of the cache. To apply most of these transformations, the compiler requires a precise knowledge of the locality of the different sections of the code, both before and after being transformed.Cache ...

Keywords: Cache memories, optimization, sampling

8 A Characterization of Ten Hidden-Surface Algorithms

Evan E. Sutherland, Robert F. Sproull, Robert A. Schumacker

January 1974 **ACM Computing Surveys (CSUR)**, Volume 6 Issue 1

Full text available: pdf(4.47 MB) Additional Information: full citation, references, citings, index terms

9 Zero-cycle loads: microarchitecture support for reducing load latency

Todd M. Austin, Gurindar S. Sohi

December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

Full text available: pdf(1.35 MB) Additional Information: full citation, references, citings, index terms

10 Exploiting fine-grain thread level parallelism on the MIT multi-ALU processor

Stephen W. Keckler, William J. Dally, Daniel Maskit, Nicholas P. Carter, Andrew Chang, Whay S. Lee

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(1.56 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Much of the improvement in computer performance over the last twenty years has come from faster transistors and architectural advances that increase parallelism. Historically, parallelism has been exploited either at the instruction level with a grain-size of a single instruction or by partitioning applications into coarse threads with grain-sizes of thousands of instructions. Fine-grain threads fill the parallelism gap between these extremes by enabling tasks with run lengths as small as 20 cyc ...

11 Delay streams for graphics hardware

Timo Aila, Ville Miettinen, Petri Nordlund

July 2003 **ACM Transactions on Graphics (TOG)**, Volume 22 Issue 3

Full text available: pdf(1.67 MB) Additional Information: full citation, abstract, references, index terms

In causal processes decisions do not depend on future data. Many well-known problems, such as occlusion culling, order-independent transparency and edge antialiasing cannot be properly solved using the traditional causal rendering architectures, because future data may change the interpretation of current events.We propose adding a *delay stream* between the vertex and pixel processing units. While a triangle resides in the delay stream, subsequent triangles generate occlusion information. ...

Keywords: 3D graphics hardware, antialiasing, occlusion culling, order-independent transparency, stream processing

12 Exploiting choice: instruction fetch and issue on an implementable simultaneous multithreading processor

Dean M. Tullsen, Susan J. Eggers, Joel S. Emer, Henry M. Levy, Jack L. Lo, Rebecca L. Stamm

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2

Full text available: pdf(1.48 MB) Additional Information: full citation, abstract, references, citings, index terms

Simultaneous multithreading is a technique that permits multiple independent threads to issue multiple instructions each cycle. In previous work we demonstrated the performance potential of simultaneous multithreading, based on a somewhat idealized model. In this paper we show that the throughput gains from simultaneous multithreading can be achieved *without* extensive changes to a conventional wide-issue superscalar, either in hardware structures or sizes. We present an architecture for s ...

13 Hybrid volume and polygon rendering with cube hardware

Kevin Kreeger, Arie Kaufman

July 1999 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.85 MB) Additional Information: full citation, references, citings, index terms

Keywords: cube architecture, mixing polygons and volumes, ray casting, run-length-encoding, volume rendering

14 Towards a Systematic, Pragmatic and Architecture-Aware Program Optimization Process for Complex Processors

David Parello, Olivier Temam, Albert Cohen, Jean-Marie Verdun

November 2004 **Proceedings of the 2004 ACM/IEEE conference on Supercomputing**

Full text available: pdf(253.48 KB) Additional Information: full citation, abstract

Because processor architectures are increasingly complex, it is increasingly difficult to embed accurate machine models within compilers. As a result, compiler efficiency tends to decrease. Currently, the trend is on top-down approaches: static compilers are progressively augmented with information from the architecture as in profile-based, iterative or dynamic compilation techniques. However, for the moment, fairly elementary architectural information is used. In this article, we adopt a bottom ...

15 Dynamic memory disambiguation for array references

David Bernstein, Doron Cohen, Dror E. Maydan

November 1994 **Proceedings of the 27th annual international symposium on Microarchitecture**

Full text available: pdf(924.07 KB) Additional Information: full citation, abstract, references, citings, index terms

Memory disambiguation, or alias analysis, is a key component of modern optimizing compilers. Any optimization that reorders or changes code containing memory operations must analyze the memory references to ensure that the original semantics of the program are not changed.The recent proliferation of machines able to exploit parallelism, either at the coarse grain or more commonly at the instruction level, has led to the development of sophisticated memory disambiguation algorithm ...

16 Improving parallel shear-warp volume rendering on shared address space multiprocessors

Dongming Jiang, Jaswinder Pal Singh

June 1997 **ACM SIGPLAN Notices , Proceedings of the sixth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 32 Issue 7

Full text available: pdf(1.30 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a new parallel volume rendering algorithm and implementation, based on shear warp factorization, for shared address space multiprocessors. Starting from an existing parallel shear-warp renderer, we use increasingly detailed performance measurements on real machines and simulators to understand performance bottlenecks. This leads us to a new parallel implementation that substantially outperforms and out-scales the old one on a range of shared address space platforms, from bus- ...

17 Steps towards an ecology of infrastructure: complex problems in design and access for large-scale collaborative systems

Susan Leigh Star, Karen Ruhleder

October 1994 **Proceedings of the 1994 ACM conference on Computer supported cooperative work**

Full text available: pdf(1.49 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper analyzes the initial phases of a large-scale custom software effort, the Worm Community System (WCS), a collaborative system designed for a geographically dispersed community of geneticists. Despite high user satisfaction with the system and interface, and extensive user feedback and analysis, many users experienced difficulties in signing on and use, ranging from simple lack of resources to complex organizational and intellectual trade-offs. Using Bateson's levels of learning, w ...

Keywords: collaboratory, ethnography, infrastructure, organizational computing,

participatory design

18 Collaborative virtual environment: DEVA3: architecture for a large-scale distributed virtual reality system

Steve Pettifer, Jon Cook, James Marsh, Adrian West

October 2000 **Proceedings of the ACM symposium on Virtual reality software and technology**

Full text available: pdf(1.52 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present work undertaken by the Advanced Interfaces Group at the University of Manchester on the design and development of a system to support large numbers of geographically distributed users in complex, large-scale virtual environments (VEs).We shown how the problem of synchronisation in the face of network limitations is being addressed by the Deva system through the exploitation of subjectivity. Further, we present a model for flexibly describing object behaviours in the VEs. ...

Keywords: Distribution, Object behavior, Programming model, Subjectivity, System architecture, Virtual Environments

19 Automating the lexical and syntactic design of graphical user interfaces: the UofA* UIMS

Gurminder Singh, Mark Green

July 1991 **ACM Transactions on Graphics (TOG)**, Volume 10 Issue 3

Full text available: pdf(3.82 MB) Additional Information: full citation, references, citings, index terms, review

20 Fragmentation considered harmful

Christopher A. Kent, Jeffrey C. Mogul

January 1995 **ACM SIGCOMM Computer Communication Review**, Volume 25 Issue 1

Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, index terms

Internetworks can be built from many different kinds of networks, with varying limits on maximum packet size. Throughput is usually maximized when the largest possible packet is sent; unfortunately, some routes can carry only very small packets. The IP protocol allows a gateway to *fragment* a packet if it is too large to be transmitted. Fragmentation is at best a necessary evil; it can lead to poor performance or complete communication failure. There are a variety of ways to reduce the lik ...

Terms used **tile conflict fragment shading stall delay** Found **44** of **160,172**

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1 Dynamically scheduled VLIW processors

B. Ramakrishna Rau

December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**

Full text available: pdf(1.64 MB) Additional Information: full citation, references, citings

Keywords: VLIW processors, dynamic scheduling, multiple operation issue, out-of-order execution, scoreboarding

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Mark J. Kilgard

August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.66 MB) Additional Information: full citation, references, citings, index terms

Keywords: O2, OpenGL, graphics hardware architecture, infinite-reality

3 A Characterization of Ten Hidden-Surface Algorithms

Evan E. Sutherland, Robert F. Sproull, Robert A. Schumacker

January 1974 **ACM Computing Surveys (CSUR)**, Volume 6 Issue 1

Full text available: pdf(4.47 MB) Additional Information: full citation, references, citings, index terms

4 Delay streams for graphics hardware

Timo Aila, Ville Miettinen, Petri Nordlund

July 2003 **ACM Transactions on Graphics (TOG)**, Volume 22 Issue 3

Full text available: pdf(1.67 MB) Additional Information: full citation, abstract, references, index terms

In causal processes decisions do not depend on future data. Many well-known problems, such as occlusion culling, order-independent transparency and edge antialiasing cannot be properly solved using the traditional causal rendering architectures, because future data may change the interpretation of current events.We propose adding a *delay stream* between the vertex and pixel processing units. While a triangle resides in the delay stream, subsequent triangles generate occlusion information. ...

Keywords: 3D graphics hardware, antialiasing, occlusion culling, order-independent transparency, stream processing

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Kevin Kreeger, Arie Kaufman

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Full text available: pdf(1.85 MB) Additional Information: full citation, references, citings, index terms

Keywords: cube architecture, mixing polygons and volumes, ray casting, run-length-encoding, volume rendering

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Todd M. Austin, Gurindar S. Sohi

December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

Full text available: pdf(1.35 MB) Additional Information: full citation, references, citings, index terms

7 Parallel texture caching

Homan Igehy, Matthew Eldridge, Pat Hanrahan

July 1999 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.80 MB) Additional Information: full citation, references, citings, index terms

8 Special issue on knowledge representation

Ronald J. Brachman, Brian C. Smith

February 1980 **ACM SIGART Bulletin**, Issue 70

Full text available: pdf(13.13 MB) Additional Information: full citation, abstract

In the fall of 1978 we decided to produce a special issue of the SIGART Newsletter devoted to a survey of current knowledge representation research. We felt that there were twe useful functions such an issue could serve. First, we hoped to elicit a clear picture of how people working in this subdiscipline understand knowledge representation research, to illuminate the issues on which current research is focused, and to catalogue what approaches and techniques are currently being developed. Secon ...

9 Prefetching in a texture cache architecture

Homan Igehy, Matthew Eldridge, Kekoa Proudfoot

August 1998 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.45 MB) Additional Information: full citation, references, citings, index terms

10 Tiled polygon traversal using half-plane edge functions

Joel McCormack, Robert McNamara

August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(96.25 KB) Additional Information: full citation, abstract, references, citings, index terms

Existing techniques for traversing a polygon generate fragments one (or more) rows or columns at a time. (A fragment is all the information needed to paint one pixel of the polygon.) This order is non-optimal for many operations. For example, most frame buffers are tiled into rectangular pages, and there is a cost associated with accessing a different page. Pixel processing is more efficient if all fragments of a polygon on one page are generated before any fragments on a different page. Si ...

Keywords: graphics accelerators, rasterization, tiling

11 High-level synthesis of distributed logic-memory architectures 
Chao Huang, Srivaths Ravi, Anand Raghunathan, Niraj K. Jha
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, index terms

With the increasing cost of global communication on-chip, high-performance designs for data-intensive applications require architectures that distribute hardware resources (computing logic, memories, interconnect, *etc.*) throughout a chip, while restricting computations and communications to geographic proximities. In this paper, we present a methodology for high-level synthesis (HLS) of distributed logic-memory architectures, *i.e.*, architectures that have logic and memory distribut ...

12 Data space-oriented tiling for enhancing locality 
I. Kadayif, M. Kandemir
May 2005 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 4 Issue 2
Full text available: pdf(978.44 KB) Additional Information: full citation, abstract, references, index terms

Improving locality of data references is becoming increasingly important due to increasing gap between processor cycle times and off-chip memory access latencies. Improving data locality not only improves effective memory access time but also reduces memory system energy consumption due to data references. An optimizing compiler can play an important role in enhancing data locality in array-intensive embedded media applications with regular data access patterns.This paper presents a compiler-bas ...

Keywords: Software compilation, array-intensive applications, data locality, iteration space tiling, scratch pad memory

13 Exploiting weak connectivity for mobile file access 
L. B. Mummert, M. R. Ebling, M. Satyanarayanan
December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles**, Volume 29 Issue 5
Full text available: pdf(1.49 MB) Additional Information: full citation, references, citings, index terms

14 A structural view of the Cedar programming environment 
Daniel C. Swinehart, Polle T. Zellweger, Richard J. Beach, Robert B. Hagmann
August 1986 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 8 Issue 4
Full text available: pdf(6.32 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

15 Virtual Memory 
Peter J. Denning
September 1970 **ACM Computing Surveys (CSUR)**, Volume 2 Issue 3
Full text available: pdf(2.63 MB) Additional Information: full citation, references, citings, index terms

Query evaluation techniques for large databases
Goetz Graefe
June 1993 **ACM Computing Surveys (CSUR)**, Volume 25 Issue 2

Full text available: pdf(9.37 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Database management systems will continue to manage large data volumes. Thus, efficient algorithms for accessing and manipulating large sets and sequences will be required to provide acceptable performance. The advent of object-oriented and extensible database systems will not solve this problem. On the contrary, modern data models exacerbate the problem: In order to manipulate large sets of complex objects as efficiently as today's database systems manipulate simple records, query-processi ...

Keywords: complex query evaluation plans, dynamic query evaluation plans, extensible database systems, iterators, object-oriented database systems, operator model of parallelization, parallel algorithms, relational database systems, set-matching algorithms, sort-hash duality

17 Data Space Oriented Scheduling in Embedded Systems
M. Kandemir, G. Chen, W. Zhang, I. Kolcu
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

Full text available: pdf(274.03 KB) Publisher Site Additional Information: full citation, abstract, index terms

With the widespread use of embedded devices such as PDAs, printers, game machines, cellular telephones, achieving high performance demands an optimized operating system (OS) that can take full advantage of the underlying hardware components. This paper presents a locality conscious process scheduling strategy for embedded environments. The objective of our scheduling strategy is to maximize reuse in the data cache. It achieves this by restructuring the process codes based on data sharing pattern ...

18 Identifying and Exploiting Spatial Regularity in Data Memory References
Tushar Mohan, Bronis R. de Supinski, Sally A. McKee, Frank Mueller, Andy Yoo, Martin Schulz
November 2003 **Proceedings of the 2003 ACM/IEEE conference on Supercomputing**

Full text available: pdf(264.75 KB) Additional Information: full citation, abstract

The growing processor/memory performance gap causes the performance of many codes to be limited by memory accesses. If known to exist in an application, strided memory accesses forming streams can be targeted by optimizations such as prefetching, relocation, remapping, and vector loads. Undetected, they can be a significant source of memory stalls in loops. Existing stream-detection mechanisms either require special hardware, which may not gather statistics for subsequent analysis, or are limite ...

19 Proceedings of the SIGNUM conference on the programming environment for development of numerical software
March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1

Full text available: pdf(5.02 MB) Additional Information: full citation

20 Modulo scheduling for the TMS320C6x VLIW DSP architecture
Eric Stotzer, Ernst Leiss
May 1999 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1999 workshop on Languages, compilers, and tools for embedded systems**, Volume 34 Issue 7

Full text available: pdf(901.18 KB) Additional Information: full citation, abstract, references, citings, index terms

Digital Signal Processing (DSP) architectures are specialized for high performance numerical algorithms such as those found in communication and multimedia applications. The development of efficient compilers for DSP processors is a growing research area. The

Texas Instruments TMS320C6x (C6x) is a Very Long Instruction Word (VLIW) DSP architecture capable of issuing eight operations in parallel. In this paper, we present the results of implementing a software pipelining algorithm for the C6x. We ...

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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Lardjane, N.; Ahmed-Nacer, M.;
Computer Systems and Applications, 2003. Book of Abstracts. ACS/IEEE International Conference on
14-18 July 2003 Page(s):44
Digital Object Identifier 10.1109/AICCSA.2003.1227477
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2. **A multi-version algorithm for cooperative edition of hierarchically-structured documents**
Ribo, J.M.; Franch, X.;
Groupware, 2001. Proceedings. Seventh International Workshop on
6-8 Sept. 2001 Page(s):154 - 163
Digital Object Identifier 10.1109/CRIWG.2001.951840
AbstractPlus | Full Text: PDF(632 KB) **IEEE CNF**

3. **Meta-context mediation to attain semantic interoperability**
Biletskiy, Y.; Campeanu, C.; Dudar, Z.; Vorochek, O.;
Intelligent Systems, 2004. Proceedings. 2004 2nd International IEEE Conference
Volume 1, 22-24 June 2004 Page(s):238 - 243 Vol.1
AbstractPlus | Full Text: PDF(554 KB) **IEEE CNF**

4. **Model-checking trace event structures**
Madhusudan, P.;
Logic in Computer Science, 2003. Proceedings. 18th Annual IEEE Symposium on
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Digital Object Identifier 10.1109/LICS.2003.1210077
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